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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/534,164	05/05/2005	Matthias Muth	DE02 0252 US	9960

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EXAMINER	
ZAMAN, FAISAL M	
ART UNIT	**PAPER NUMBER**
2111	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/534,164	MUTH, MATTHIAS	
	Examiner	Art Unit	
	Faisal Zaman	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1 and 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Feuerstraeter et al. ("Feuerstraeter") (U.S. Patent Application Publication No. 2003/0058894), Applicant's Admitted Prior Art (hereinafter "AAPA"), and Ishikuri (U.S. Patent No. 6,674,681).

Regarding Claim 1, AAPA teaches that to enable synchronization between two communicating devices using a LIN protocol, the receiving device would need to be capable of recognizing certain symbols that differ from those employed by a standard interface (AAPA, Page 1, lines 9-16).

AAPA does not expressly teach an integrated circuit having a system base chip that has basic functions for a transmitting and/or receiving system for a vehicle data bus, namely at least a system voltage supply, a system reset, and a monitoring function, an interface circuit that, in a self-contained fashion, runs at least parts of a data bus protocol that performs detection of the bit-rate of received data, and that is capable of passing on at least one received or transmitted byte, and a serial/parallel converter that makes use in its conversion of the bit-rate detected by the interface circuit.

In the same field of endeavor (e.g. detection of data transfer rates in a bus system), Feuerstraeter teaches an integrated circuit having

A system base chip (Feuerstraeter, Figure 3, item 340) that has basic functions for a transmitting and/or receiving system for a data bus, namely at least a monitoring function (Feuerstraeter, Figure 7, item 700),

An interface circuit that, in a self-contained fashion, runs at least parts of a data bus protocol that performs detection of the bit-rate of received data, and that is capable of passing on at least one received or transmitted byte (Feuerstraeter, Figure 4, item 420, Page 4, paragraphs 0044 and 0047),

A serial/parallel converter that makes use in its conversion of the bit-rate detected by the interface circuit (Feuerstraeter, Figure 3, items 350/360, Page 3, paragraph 0037).

Also in the same field of endeavor (e.g. transmitting and receiving data in an integrated circuit), Ishikuri teaches an integrated circuit having a system voltage supply (Ishikuri, Figure 1, item 1, Column 5, lines 43-56), and

A system reset (Ishikuri, Column 5, lines 57-60).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Feuerstraeter's teachings of detection of data transfer rates in a bus system with the teachings of AAPA, for the purpose of automatically detecting a data transfer rate such that one or more devices may communicate with each other when otherwise the devices would not (see Feuerstraeter, Page 1, paragraph 0011). It also would have been obvious to one of ordinary skill in the

art at the time the invention was made to have combined Ishikuri's teachings of transmitting and receiving data in an integrated circuit with the teachings of AAPA, for the purpose of preventing erroneous operations due to runaway of a system (see Ishikuri, Column 5, lines 6-8).

Regarding Claim 6, AAPA teaches the use of an SCI/UART (Serial Communication Interface/Universal Asynchronous Receiver Transmitter) interface (AAPA, Page 1, lines 13-17).

The motivation that was used in the combination of Claim 1, super, applies equally as well to Claim 6.

3. **Claims 2 and 3** are rejected under 35 U.S.C. 103(a) as being unpatentable over Feuerstraeter, AAPA, and Ishikuri as applied to claim 1 above (hereinafter "FAI"), and further in view of Bongiorno et al. ("Bongiorno") (U.S. Patent No. 6,292,045).

Regarding Claim 2, FAI teaches an oscillator that acts as a clock-signal source and as a timebase for the bit-rate detection (Feuerstraeter, Figure 3, items 480/490, Page 4, paragraph 0044).

FAI does not expressly teach wherein the oscillator is an R/C oscillator.

In the same field of endeavor (e.g. electrical circuits which use clock sources), Bongiorno teaches the use of an R/C oscillator (Bongiorno, Column 1, lines 16-21).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Bongiorno's teachings of electrical

circuits which use clock sources with the teachings of FAI, for the purpose of providing an RC oscillator which has the ability to generate high frequency oscillations having a stable frequency characteristic.

Regarding Claim 3, Bongiorno teaches wherein the clock signal generated by the R/C oscillator may also be provided to circuits outside the integrated circuit, and in particular to a microprocessor (Bongiorno, Column 1, lines 16-21).

The motivation that was used in the combination of Claim 2, super, applies equally as well to Claim 3.

4. **Claims 4 and 5** are rejected under 35 U.S.C. 103(a) as being unpatentable over FAI, and further in view of Werle (U.S. Patent No. 5,778,002).

Regarding Claims 4 and 5, FAI does not expressly teach wherein the interface circuit may also pass on complete messages and perform buffer-storage of data received or to be transmitted.

In the same field of endeavor (e.g. multiplexing asynchronous high-speed and low-speed data into a single data stream for recordation), Werle teaches wherein an interface circuit may pass on complete messages by performing buffer-storage of data received or to be transmitted (Werle, Figure 1, item 14, Column 3, lines 13-27).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Werle's teachings of multiplexing asynchronous high-speed and low-speed data into a single data stream for recordation

with the teachings of FAI, for the purpose of reducing latency of the system if the incoming data rate is slower than that which can be processed.

Prior Art of Record

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Pohlmeyer et al. (U.S. Patent No. 6,959,014) discloses automatic baud rate detection in a LIN protocol bus.

Response to Arguments

6. Applicant's arguments filed 2/9/2007 have been fully considered but they are not persuasive.

Regarding Claim 1, Applicant argues that the proposed modifications "would replace Feuerstraeter's WAN/LAN dual communications approach with a dedicated LIN protocol system and, correspondingly, frustrate Feuerstraeter's purpose of selectively communicating over both WAN and LAN networks with a particular port", and further that "the Section 103(a) rejections of claim 1-6 are improper". The examiner respectfully disagrees. Contrary to Applicant's argument, incorporating the automatic baud rate detection system of Feuerstraeter into the LIN bus system of AAPA would in fact be proper. AAPA teaches that to enable synchronization between two communicating devices, the receiving device would need to be capable of recognizing certain symbols that differ from those employed by a standard interface. The disclosure of Feuerstraeter would however alleviate this problem, due it's ability to automatically detect a data

transfer rate such that one or more devices may communicate with each other when otherwise the devices would not, see Page 1, paragraph 0011. In order to accomplish this, Feuerstraeter teaches the use of serializers, deserializers, data rate detection units, and frequency selectors, among other components, as described in the rejection of Claim 1 above. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Also with regards to Claim 1, Applicant argues that "[t]he Office Action has further failed to show how the PMA layer 340 carries out monitoring functions in item 700 in Fig. 7 of the Feuerstraeter reference". The examiner respectfully disagrees. Contrary to Applicant's argument, as can be seen in Page 6, paragraph 0063, item 700 of Figure 7 is referring to "where an incoming data stream is detected at the input of the deserializer." Deserializer 360 is shown in Figure 3 as being a part of PMA 340, and thus item 700 does in fact correspond to PMA 340.

Further with regards to Claim 1, Applicant argues that "not only does the POC circuit 1 [of Ishikuri] fail to correspond to the claimed system voltage supply, it requires and operates with a separate system voltage supply and thus requires external

functionality, teaching away from the claimed invention." The examiner respectfully disagrees. Contrary to Applicant's argument, the POC 1 of does in fact teach both the "system voltage supply" and "system reset" of Claim 1, as can be seen in Figure 1 of Ishikuri, and further in Column 5, lines 43-60. With regards to the fact that the system voltage supply of Ishikuri requires external functionality, the examiner notes that this is exactly how the system voltage supply of the present application functions, as can be seen in Figure 1 of the present application, where a car battery (BAT) provides the voltage supply to the voltage controller 3, which in turns provides power to microcontroller 7.

Finally with regards to Claim 1, Applicant argues that "a data rate detection unit 420 detects an incoming data stream, but does not appear to pass on any received or transmitted bytes, and further is limited to operation with a WAN or LAN protocol." The examiner respectfully disagrees. Contrary to Applicant's argument, the data rate detection unit 420 does in fact teach passing on received or transmitted bytes. As can be seen in Figure 4 of Feuerstraeter, incoming data stream 415 is shown as going from PMD to PCS, while only the phase rate of the incoming data stream is sampled at data rate detection unit 420 (ie. the remaining incoming data stream is passed on through to PCS), see Page 4, paragraph 0044. Therefore, the data rate detection unit 420 does in fact pass on received or transmitted bytes as claimed.

Therefore, the claims stand as previously rejected.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Faisal Zaman whose telephone number is 571-272-6495. The examiner can normally be reached on Monday thru Friday, 8 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FMZ

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